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EIA/JESD54

# EIA/JEDEC STANDARD

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**Standard for Description of  
54/74ABTXXX and 74BCXXX  
TTL-Compatibility BiCMOS Logic  
Devices**

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**EIA/JESD54**

**FEBRUARY 1996**

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**ELECTRONIC INDUSTRIES ASSOCIATION  
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**Standard for Description of  
54/74ABTXXX and 74BCXXX  
TTL-Compatible BiCMOS Logic Devices**

(From JEDEC Council ballot JCB-95-67, formulated under the cognizance of JC-40 Committee on Standardization of Digital Logic.)

## CONTENTS

Section	Page
<b>1 PURPOSE AND SCOPE</b>	<b>1</b>
1.1 Purpose	1
1.2 Scope	1
<b>2 DEFINITIONS</b>	<b>1</b>
<b>3 STANDARD SPECIFICATIONS</b>	<b>2</b>
3.1 Absolute Maximum Continuous Ratings	2
3.2 Recommended Operating Conditions	2
3.3 ABT DC Specifications	3
3.4 BC DC Specifications	4
<b>4 TEST CIRCUITS AND SWITCHING WAVEFORMS</b>	<b>5</b>
<b>5 SUPPLY CURRENT TEST PROCEDURES</b>	<b>12</b>
<b>6 ABT SWITCHING SPEED STANDARDS</b>	<b>13</b>
6.1 Index of Device Types	13
6.2 Switching Speed Tables	14
<b>7 BC SWITCHING SPEED STANDARDS</b>	<b>29</b>
7.1 Index of Device Types	29
7.2 Switching Speed Tables	30

## 1 PURPOSE AND SCOPE

### 1.1 Purpose:

To provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

### 1.2 Scope:

This standard covers specifications for BiCMOS Logic series as defined in Section 2.

## 2 DEFINITIONS

### BiCMOS Series

Includes devices combining bipolar and silicon-gate complementary metal-oxide-semiconductor (CMOS) field effect devices in a single-chip integrated circuit.

### ABTXXXXXX Series

Includes devices whose input logic levels are TTL compatible, whose outputs are specified at TTL levels.

### BCXXX Series

Includes devices whose input logic levels are TTL compatible, whose outputs are specified at TTL levels and the output sink current is specified at either 24mA or 48mA.

### Prefixes

Prefixes "54" or "74" immediately preceding "ABT" or "BC" indicate the operating temperature range. For example, 54ABTXXXXXX refers to the Military (MIL) version of devices which are specified over the temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . 74BCXXX or 74ABTXXXXXX refers to the Commercial (COM'L) version of devices which are specified over the temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### 3 STANDARD SPECIFICATIONS

#### 3.1 Absolute Maximum Continuous Ratings (Notes 1 and 2):

Supply Voltage, $V_{CC}$	–0.5 V to 7 V
dc input voltage, $V_I$ (Note 3)	–0.5 V to $V_{CC}$
dc output voltage, $V_O$	–0.5 V to 5.5 V
dc input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
dc output clamp current, $I_{OK}$ ( $V_O < 0$ )	–30 mA
dc current into any output in the low state, $I_{OL}$ (Note 4)	$2 \times I_{OL(rated)}$
dc current into any output in the high state, $I_{OH}$ (Note 5)	$2 \times I_{OH(rated)}$
Storage temperature range	–65°C to 150°C

Note 1: Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

Note 2: Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

Note 3: The dc input voltage rating may be exceeded if the dc input clamp current ratings are observed.

Note 4: Not to exceed 70 mA.

Note 5: Not to exceed –35 mA.

#### 3.2 Recommended Operating Conditions:

Symbol	Parameter		MIN	NOM	MAX	Unit
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>I</sub>	Input Voltage		0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0		V <sub>CC</sub>	V
T <sub>A</sub>	Operating free-air temperature	74 Series	−40	25	85	°C
		54 Series	−55	25	125	°C
ΔV/Δv	Input transition rise or fall rate (Note 1)		0		5	ns/V

Note 1: As measured between 0.8 V and 2 V.

### 3.3 ABT dc Specifications:

Symbol	Parameter	Test Conditions	54/74 Series		Unit
			MIN	MAX	
$V_{IH}$	High-level input voltage		2		V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$		-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3 \text{ mA}$	2.4	V
			$I_{OH} = -12 \text{ mA}$	2	V
			$I_{OH} = -24 \text{ mA}, (\text{Note } 5)$	2	V
			$I_{OH} = -32 \text{ mA}, (\text{Notes } 4,5)$	2	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$	0.8	V
			$I_{OL} = 48 \text{ mA}, (\text{Note } 5)$	0.55	V
			$I_{OL} = 64 \text{ mA}, (\text{Notes } 4,5)$	0.55	V
$I_I$	Input current	$V_{CC} = \text{MAX},$ $V_I = V_{CC}$	except I/O ports	0.1	mA
			I/O ports	1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX},$ $V_I = 2.7 \text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX},$ $V_I = 0.5 \text{ V}$		-10	$\mu\text{A}$
$I_{OZH}$	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 2.7 \text{ V}$	except I/O ports	50	$\mu\text{A}$
			I/O ports	60	$\mu\text{A}$
$I_{OZL}$	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 0.5 \text{ V}$	except I/O ports	-50	$\mu\text{A}$
			I/O ports	-60	$\mu\text{A}$
$I_{OS}$	Output short-circuit current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0$	-50		mA
$I_{CCZ}$	Static supply current, outputs high-impedance	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	$\mu\text{A}$
$I_{CCH}$	Static supply current, outputs high	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	$\mu\text{A}$
$I_{CCL}$	Static supply current outputs low	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	mA
$\Delta I_{CC}$	Static supply current per input at TTL levels	$V_I = V_{CC} - 2.1 \text{ V or } V_I = 0.5 \text{ V},$ $V_{CC} = \text{MIN to MAX}$		2.5	mA

Note 1: For I/O pins,  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

Note 2: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 3: Refer to manufacturer's datasheets.

Note 4: Not applicable to 54 series products.

Note 5: Not applicable to series resistor parts.

## 3.4 BC dc Specifications:

Symbol	Parameter	Test Conditions	74 Series		Unit
			MIN	MAX	
$V_{IH}$	High-level input voltage		2		V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$		-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3 \text{ mA}$	2.4	V
			$I_{OH} = -15 \text{ mA}$	2	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24 \text{ mA}$	0.55	V
			$I_{OL} = 48 \text{ mA}$	(Note 3)	V
$I_I$	Input current	$V_{CC} = \text{MAX},$ $V_I = V_{CC}$	except I/O ports	1	$\mu\text{A}$
			I/O ports	1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX},$ $V_I = 2.7 \text{ V}$	except I/O ports	1	$\mu\text{A}$
			I/O ports	50	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX},$ $V_I = 0.5 \text{ V}$	except I/O ports	-1	$\mu\text{A}$
			I/O ports	-50	$\mu\text{A}$
$I_{OZH}$	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 2.7 \text{ V}$		50	$\mu\text{A}$
$I_{OZL}$	Off-state output current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0.5 \text{ V}$		-50	$\mu\text{A}$
$I_{OS}$	Output short-circuit current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0$	-60		mA
$I_{CCZ}$	Static supply current, outputs high-impedance	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		50	$\mu\text{A}$
$I_{CCH}$	Static supply current, outputs high	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		50	$\mu\text{A}$
$I_{CCL}$	Static supply current outputs low	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		(Note 3)	mA
$\Delta I_{CC}$	Static supply current per input at TTL levels	$V_I = V_{CC} - 2.1 \text{ V or } V_I = 0.5 \text{ V},$ $V_{CC} = \text{MIN to MAX}$		1.5	mA

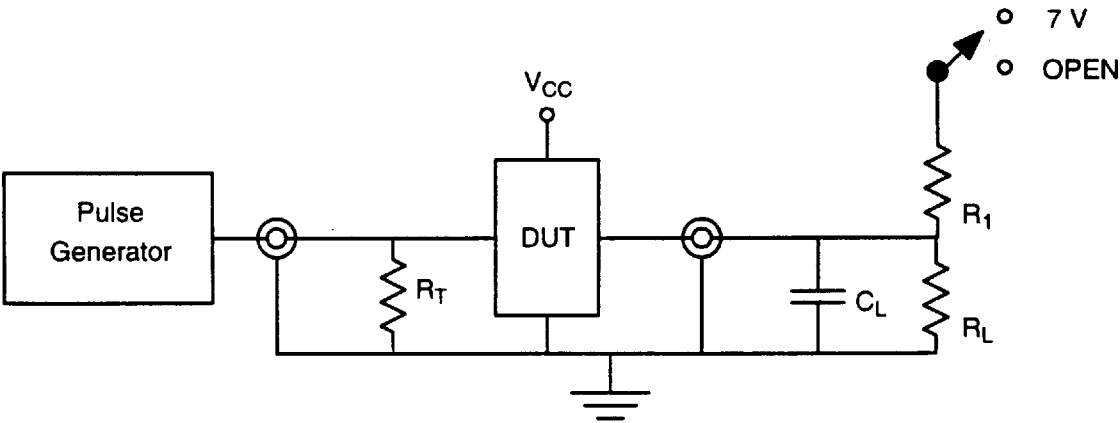
Note 1: For I/O pins,  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

Note 2: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 3: Refer to manufacturer's datasheets.



4 TEST CIRCUITS AND SWITCHING WAVEFORMS

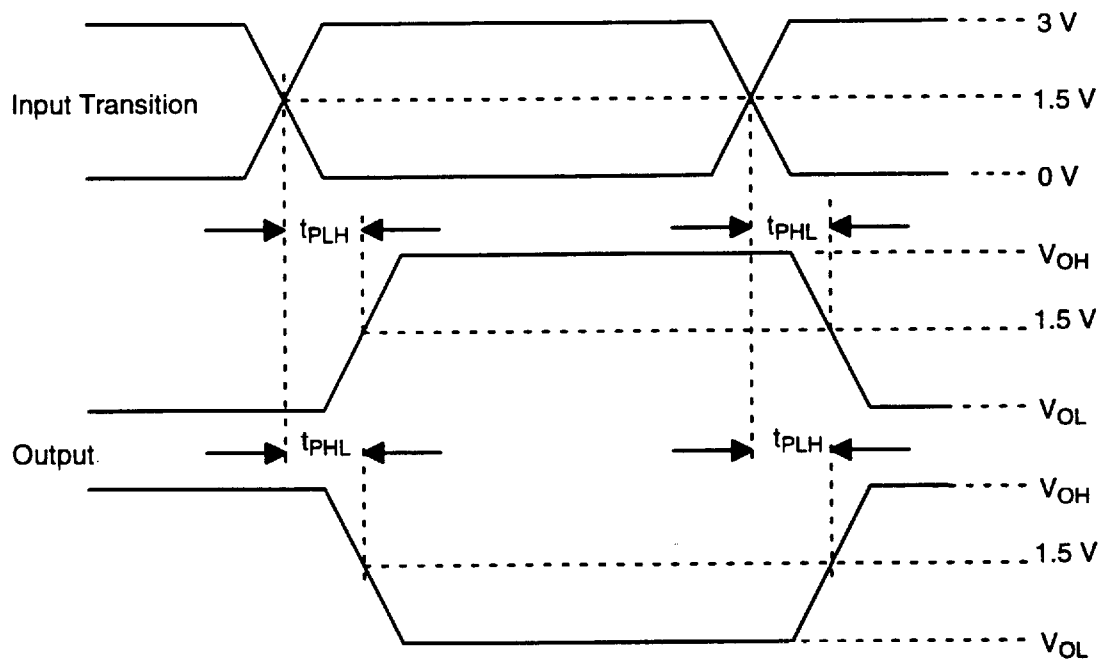
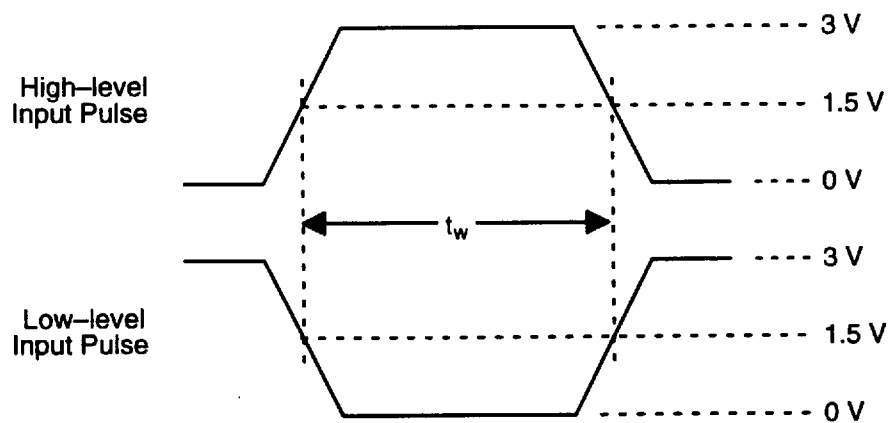


Test	Switch
$t_{PLH}$ (except open-collector outputs)	Open
$t_{PLH}$ (open-collector outputs)	7 V
$t_{PHL}$ (except open-collector outputs)	Open
$t_{PHL}$ (open-collector outputs)	7 V
$t_{PZH}$	Open
$t_{PZL}$	7 V
$t_{PHZ}$	Open
$t_{PLZ}$	7 V

$C_L = 50 \text{ pF}$  or equivalent (includes jig and probe capacitance)

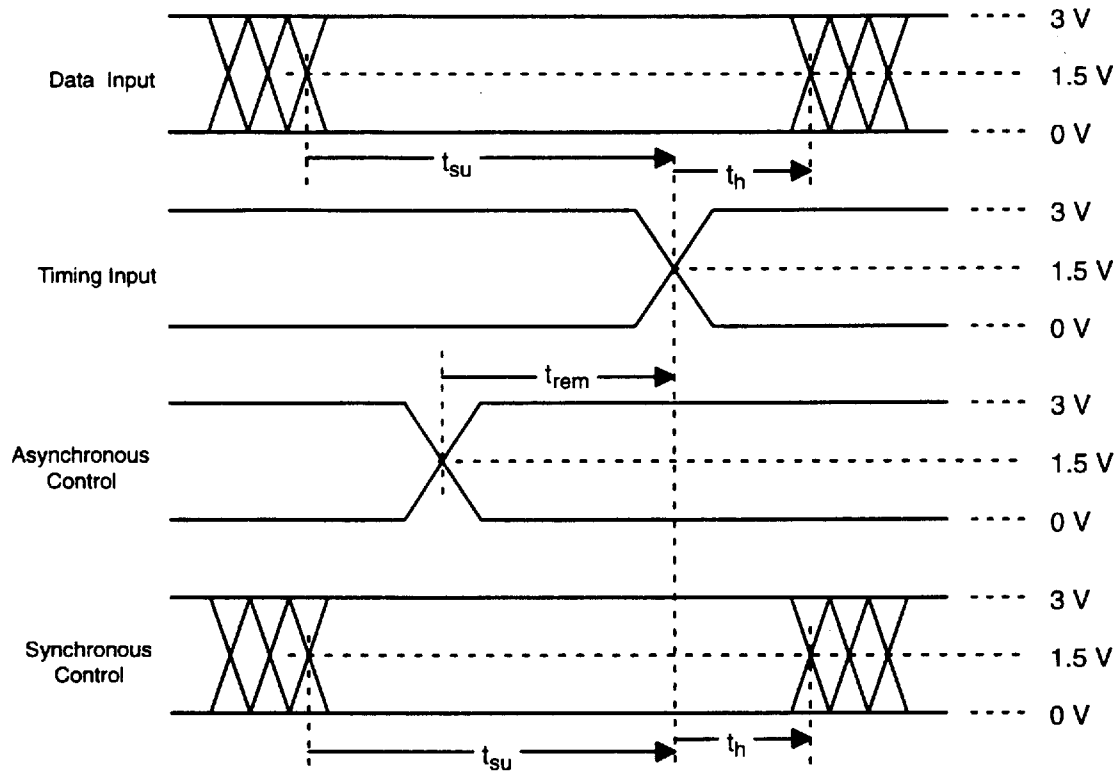
$R_L = R_1 = 500 \text{ } \Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50 \text{ } \Omega$ )

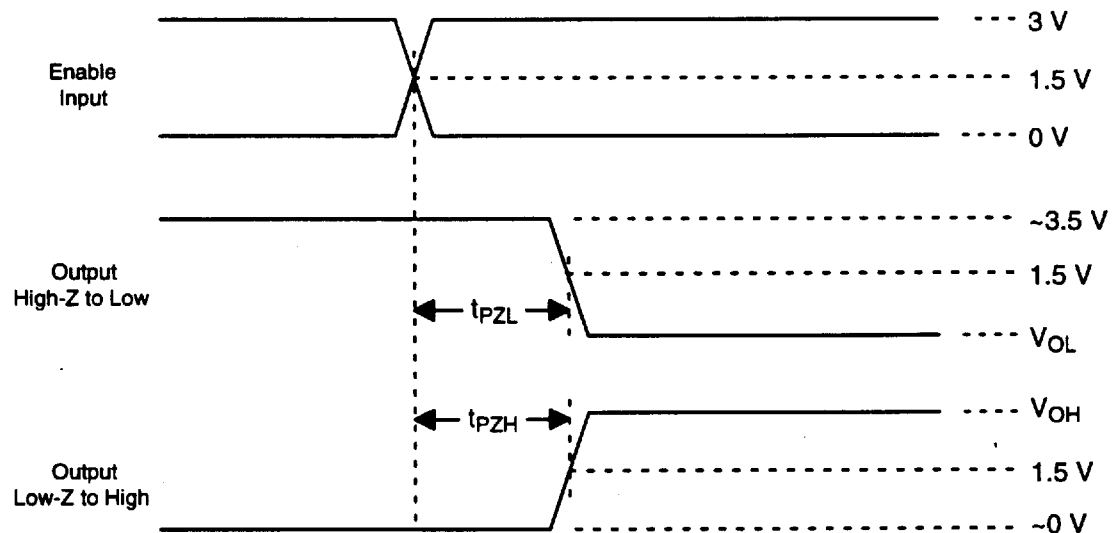
**PROPAGATION DELAY MEASUREMENTS****PULSE DURATION (WIDTH) MEASUREMENTS**

- Output requirements: Device must follow truth table  
 $V_{OL} \leq 0.8 \text{ V}$   
 $V_{OH} \geq 2.0 \text{ V}$   
 Standard output loading;  $R_L = 500 \Omega$ ,  $C_L = 50 \text{ pF}$
- Input Conditions:  $t_r = t_f = 2.5 \text{ ns}$  (or as fast as required) from 10% to 90% of 0 V to 3 V.

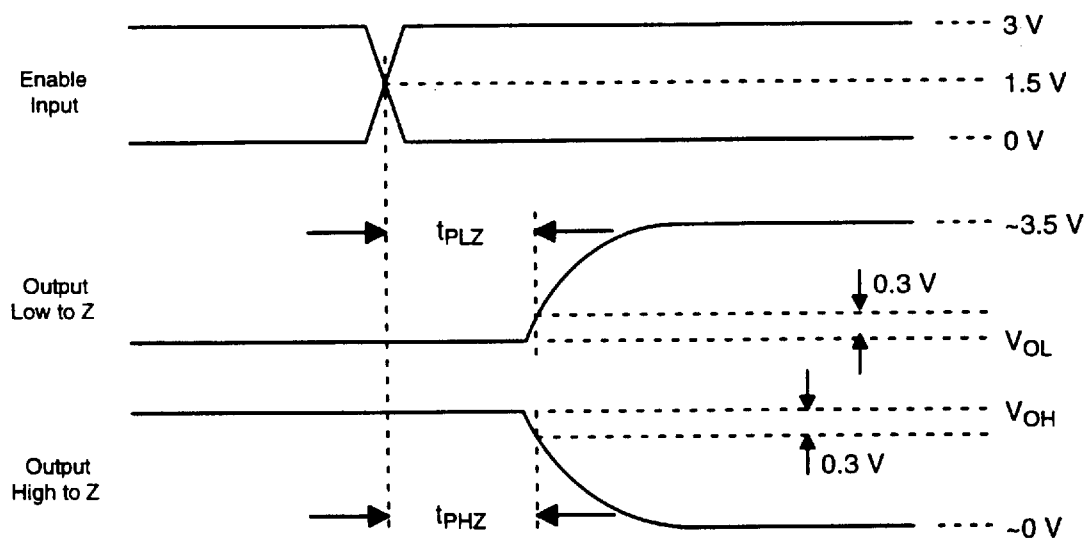
### SETUP AND HOLD TIME MEASUREMENTS



### ENABLE TIME MEASUREMENTS



### DISABLE TIME MEASUREMENTS



## 5 SUPPLY CURRENT TEST PROCEDURES

This section contains the test measurement procedure and test conditions to be used when measuring  $I_{CCL}$  on BiCMOS logic devices. A description of the symbols used follows the table. Refer to Sections 3.3 and 3.4 for other  $I_{CC}$  measurement parameters.

Device	Pin Number																											
	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
125	L	L	O	L	L	O	G	O	L	L	O	L	L	M														
126	H	L	O	H	L	O	G	O	L	H	O	L	H	M														
240,2240(240-1)	L	H	O	H	O	H	O	H	O	G	H	O	H	O	H	O	H	O	L	M								
241	L	L	O	L	O	L	O	L	O	G	L	O	L	O	L	O	L	O	H	M								
244,2244(244-1)	L	L	O	L	O	L	O	L	O	G	L	O	L	O	L	O	L	O	L	M								
245	A to B	H	L	L	L	L	L	L	L	G	O	O	O	O	O	O	O	O	L	M								
	B to A	L	O	O	O	O	O	O	O	G	L	L	L	L	L	L	L	L	L	M								
273		H	O	L	L	O	O	L	L	O	G	C	O	L	L	O	O	L	L	O	M							
373		L	O	L	L	O	O	L	L	O	G	H	O	L	L	O	O	L	L	O	M							
374		L	O	L	L	O	O	L	L	O	G	C	O	L	L	O	O	L	L	O	M							
377		L	O	L	L	O	O	L	L	O	G	C	O	L	L	O	O	L	L	O	M							
533		L	O	H	H	O	O	H	H	O	G	H	O	H	H	O	O	H	H	O	M							
534		L	O	H	H	O	O	H	H	O	G	C	O	H	H	O	O	H	H	O	M							
540		L	H	H	H	H	H	H	H	H	G	O	O	O	O	O	O	O	L	M								
541		L	L	L	L	L	L	L	L	L	G	O	O	O	O	O	O	O	L	M								
543	A to B	L	H	L	L	L	L	L	L	L	L	G	L	L	O	O	O	O	O	O	O	O	L	M				
	B to A	L	L	O	O	O	O	O	O	O	L	G	H	L	L	L	L	L	L	L	L	L	L	M				
544	A to B	L	H	H	H	H	H	H	H	H	L	G	L	L	O	O	O	O	O	O	O	L	M					
	B to A	L	L	O	O	O	O	O	O	O	L	G	H	L	H	H	H	H	H	H	H	H	L	M				
573		L	L	L	L	L	L	L	L	L	G	H	O	O	O	O	O	O	O	M								
574		L	L	L	L	L	L	L	L	L	G	C	O	O	O	O	O	O	O	M								
620	A to B	H	H	H	H	H	H	H	H	H	G	O	O	O	O	O	O	O	H	M								
	B to A	L	O	O	O	O	O	O	O	O	G	H	H	H	H	H	H	H	L	M								
623	A to B	H	L	L	L	L	L	L	L	L	G	O	O	O	O	O	O	O	H	M								
	B to A	L	O	O	O	O	O	O	O	O	G	L	L	L	L	L	L	L	L	M								
640	A to B	H	H	H	H	H	H	H	H	H	G	O	O	O	O	O	O	O	L	M								
	B to A	L	O	O	O	O	O	O	O	O	G	H	H	H	H	H	H	H	L	M								

Note: The above symbols are interpreted as follows:

H =  $V_{CC}$

L = GND (0 V)

M = Force  $V_{CC}$  / Measure  $I_{CC}$

C = Clock pulse   $\begin{matrix} \text{---} & 3\text{ V} \\ \text{---} & \text{GND} \end{matrix}$

X = Don't care;  $V_{CC}$  or GND, but not switching

G = GND (0 V)

O = Open

Device		Pin Number																											
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
646	A to B	X	L	H	L	L	L	L	L	L	L	L	G	O	O	O	O	O	O	O	O	L	X	X	M				
	B to A	X	L	L	O	O	O	O	O	O	O	O	G	L	L	L	L	L	L	L	L	L	X	M					
648	A to B	X	L	H	H	H	H	H	H	H	H	H	G	O	O	O	O	O	O	O	O	L	X	X	M				
	B to A	X	L	L	O	O	O	O	O	O	O	O	G	H	H	H	H	H	H	H	H	L	L	X	M				
651	A to B	X	L	H	H	H	H	H	H	H	H	H	G	O	O	O	O	O	O	O	O	H	X	X	M				
	B to A	X	X	L	O	O	O	O	O	O	O	O	G	H	H	H	H	H	H	H	H	L	X	M					
652	A to B	X	L	H	L	L	L	L	L	L	L	L	G	O	O	O	O	O	O	O	O	H	X	X	M				
	B to A	X	X	L	O	O	O	O	O	O	O	O	G	L	L	L	L	L	L	L	L	H	L	X	M				
657	A to B	H	L	L	L	L	L	M	L	L	L	L	O	O	O	O	O	O	G	G	O	O	O	O	L				
	B to A	L	O	O	O	O	O	M	O	O	O	H	O	L	L	L	L	L	G	G	L	L	L	L	L				
821		L	L	L	L	L	L	L	L	L	L	L	G	C	O	O	O	O	O	O	O	O	O	M					
823		L	L	L	L	L	L	L	L	L	L	H	G	C	L	O	O	O	O	O	O	O	O	M					
827		L	L	L	L	L	L	L	L	L	L	L	G	L	O	O	O	O	O	O	O	O	O	M					
833	A to B	H	L	L	L	L	L	L	L	L	O	X	G	X	L	O	O	O	O	O	O	O	O	M					
	B to A	L	O	O	O	O	O	O	O	O	O	H	G	C	H	O	L	L	L	L	L	L	L	M					
841		L	L	L	L	L	L	L	L	L	L	L	G	H	O	O	O	O	O	O	O	O	O	M					
843		L	L	L	L	L	L	L	L	L	L	H	G	H	H	O	O	O	O	O	O	O	O	M					
853	A to B	H	L	L	L	L	L	L	L	L	O	X	G	X	L	O	O	O	O	O	O	O	O	M					
	B to A	L	O	O	O	O	O	O	O	O	O	H	G	L	H	O	L	L	L	L	L	L	L	M					
861	A to B	H	L	L	L	L	L	L	L	L	L	L	G	L	O	O	O	O	O	O	O	O	O	M					
	B to A	L	O	O	O	O	O	O	O	O	O	O	G	H	L	L	L	L	L	L	L	L	L	M					
863	A to B	H	L	L	L	L	L	L	L	L	L	H	G	L	L	O	O	O	O	O	O	O	O	M					
	B to A	L	O	O	O	O	O	O	O	O	O	L	G	H	H	L	L	L	L	L	L	L	L	M					
899	A to B	L	O	H	L	L	L	L	L	L	L	L	H	G	O	L	X	O	O	O	O	O	O	O	O	O	O	L	M
	B to A	L	O	L	O	O	O	O	O	O	O	O	L	G	O	L	H	L	L	L	L	L	L	L	L	L	H	M	
2952	A to B	O	O	O	O	O	O	O	O	L	C	L	G	L	X	H	L	L	L	L	L	L	L	M					
	B to A	L	L	L	L	L	L	L	L	H	X	L	G	L	C	L	O	O	O	O	O	O	O	M					
2953	A to B	O	O	O	O	O	O	O	O	L	C	L	G	L	X	H	H	H	H	H	H	H	H	M					
	B to A	H	H	H	H	H	H	H	H	H	X	L	G	L	C	L	O	O	O	O	O	O	O	M					

Note: The above symbols are interpreted as follows:

H =  $V_{CC}$

L = GND (0 V)

M = Force  $V_{CC}$  / Measure  $I_{CC}$

C = Clock pulse  -- 3 V  
-- GND

X = Don't care;  $V_{CC}$  or GND, but not switching

G = GND (0 V)

O = Open

Device		Pin Number																											
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
16244		L	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L	L	L	L	G
		L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	L								
16245	A to B	H	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	H	L	L	L	G
		L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	L								
	B to A	L	L	L	G	L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	L	O	O	G	
		O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L								
16373		L	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L	H	L	L	G
		L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	H								
16374		L	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L	C	L	L	G
		L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	C								
16500	A to B	H	H	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	H	X	
		G	X	O	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	O	X	G	
	B to A	L	X	O	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	O	L	H	
		G	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	G	
16501	A to B	H	H	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	H	X	
		G	X	O	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	O	X	G	
	B to A	L	X	O	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	O	L	H	
		G	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	G	
16540		L	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L	L	H	H	G
		H	H	M	H	H	G	H	H	H	H	G	H	H	M	H	H	G	H	H	L								
16541		L	O	O	G	O	O	M	O	O	G	O	O	O	O	G	O	O	M	O	O	G	O	O	L	L	L	L	G
		L	L	M	L	L	G	L	L	L	L	G	L	L	M	L	L	G	L	L	L								

Device		Pin Number																											
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
16543	A to B	L	L	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	L	L	
		H	L	L	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	L	L	H	
	B to A	H	L	L	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	L	L	H	
		L	L	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	L	L	
16646	A to B	H	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	H	
		L	X	X	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	X	X	L	
	B to A	L	X	L	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	L	X	L	
		L	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	L	
16652	A to B	H	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	H	
		H	X	X	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	X	X	H	
	B to A	L	X	X	G	O	O	O	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	X	X	L	
		H	X	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	X	H	
16952	A to B	L	C	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	C	L	
		H	X	L	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	L	X	H	
	B to A	H	X	L	G	O	O	M	O	O	O	G	O	O	O	O	O	G	O	O	O	M	O	O	G	L	X	H	
		L	C	L	G	L	L	M	L	L	L	G	L	L	L	L	L	G	L	L	L	M	L	L	G	L	C	L	

Note: The above symbols are interpreted as follows:

H =  $V_{CC}$

L = GND (0 V)

M = Force  $V_{CC}$  / Measure  $I_{CC}$

C = Clock pulse  -- 3 V  
-- GND

X = Don't care;  $V_{CC}$  or GND, but not switching

G = GND (0 V)

O = Open



## **6 ABT SWITCHING SPEED STANDARDS**

This section establishes standard maximum limits for switching parameters and minimum limits for timing parameters for the device types listed herein. For parameter measurement information, refer to Section 4.

Refer to individual manufacturers' datasheets for applicable minimum limits for switching parameters.

Standardized limits for switching parameters (dynamic characteristics) are specified by part identifiers in numeric order.

### **6.1 Index of ABT device types:**

#### **6.1.1 Buffers and Drivers:**

125, 126, 240, 2240(240-1), 241, 244, 2244(244-1), 540, 541, 827, 16244, 16540, 16541

#### **6.1.2 Latches and Flip-Flops:**

273, 373, 374, 377, 533, 534, 573, 574, 821, 823, 841, 843, 16373, 16374

#### **6.1.3 Transceivers:**

245, 620, 623, 640, 861, 863, 16245

#### **6.1.4 Registered Transceivers:**

543, 544, 646, 648, 651, 652, 2952, 2953, 16500, 16501, 16543, 16646, 16652, 16952

#### **6.1.5 Transceivers with Parity:**

657, 833, 853, 899

**6.2 ABT Switching speed tables:****6.2.1 Buffers and Drivers:**

Device	Symbol	Parameter	74 Series	54 Series	Units
125	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	5.9		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, G to Y	7.4		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, G to Y	6.3		ns
126	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	6.3		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, G to Y	6.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, G to Y	6.8		ns
240	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.8		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6.2		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	6.4		ns
2240 (240-1)	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	8.4		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	6.7		ns
241	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, G or $\bar{G}$ to Y	6.8		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, G or $\bar{G}$ to Y	7.1		ns
244	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.6	5.3	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6.1	7.9	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	6.6	7.9	ns
2244 (244-1)	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	5.6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	8.3		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	6.7		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
540	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.8		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6.4		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	7.3		ns
541	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6.4		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	8.8		ns
827	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.8		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	8.6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	7.2		ns
16244	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.1		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6.3		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	6.7		ns
16540	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.3		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	5.9		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	5.3		ns
16541	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	4.2		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	5.1		ns

## 6.2.2 Latches and Flip-Flops:

Device	Symbol	Parameter	74 Series	54 Series	Units	
273	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q		7.3		ns
	t <sub>PHL</sub>	Maximum propagation delay, CLR to Q		7.4		ns
	t <sub>rem</sub>	Minimum removal time	D before CLK↑	2.5		ns
			CLR inactive before CLK↑	2		ns
	t <sub>h</sub>	Minimum hold time, D after CLK↑		1.2		ns
	t <sub>w</sub>	Minimum pulse duration	CLK high or low	3.3		ns
			CLR low	3.3		ns
373	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay	D to Q	6.2	7.2	ns
			LE to Q	7.2	7.8	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\overline{G}$ to Q		6.7	7.2	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\overline{G}$ to Q		8.2	8.2	ns
	t <sub>su</sub>	Minimum setup time, D before LE↓		1.9	2.8	ns
	t <sub>h</sub>	Minimum hold time, D after LE↓		1	2.5	ns
	t <sub>w</sub>	Minimum pulse duration, LE high		3.3	3.3	ns
374	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q		7.1	7.6	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\overline{G}$ to Q		6.7	7.2	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\overline{G}$ to Q		8.2	7.2	ns
	t <sub>su</sub>	Minimum setup time, D before CLK↑		1.5	2.5	ns
	t <sub>h</sub>	Minimum hold time, D after CLK↑		1	2.5	ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low		3.3	3.3	ns
377	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q		7.3		ns
	t <sub>su</sub>	Minimum setup time	D before CLK↑	2		ns
			CLKEN before CLK↑	3		ns
	t <sub>h</sub>	Minimum hold time	D after CLK↑	1.8		ns
			CLKEN after CLK↑	1.8		ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low		3.3		ns
533	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay	D to $\overline{Q}$	6.6		ns
			LE to $\overline{Q}$	7.3		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\overline{G}$ to Q		6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\overline{G}$ to Q		6.9		ns
	t <sub>su</sub>	Minimum setup time, D before LE↑		2.1		ns
	t <sub>h</sub>	Minimum hold time, D after LE↑		1.5		ns
	t <sub>w</sub>	Minimum pulse duration, LE high or low		3.3		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
534	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to $\bar{Q}$	7.6		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to $\bar{Q}$	6.8		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to $\bar{Q}$	7.3		ns
	t <sub>su</sub>	Minimum setup time, D before CLK $\uparrow$	2.2		ns
	t <sub>h</sub>	Minimum hold time, D after CLK $\uparrow$	0.5		ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low	3.5		ns
573	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay			
		D to Q	6.2		ns
		LE to Q	7.2		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to Q	6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to Q	6.9		ns
	t <sub>su</sub>	Minimum setup time, D before LE $\downarrow$	1.9		ns
	t <sub>h</sub>	Minimum hold time, D after LE $\downarrow$	1		ns
	t <sub>w</sub>	Minimum pulse duration, LE high	3.3		ns
574	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q	7.1		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to Q	8.6		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to Q	7		ns
	t <sub>su</sub>	Minimum setup time, D before CLK $\uparrow$	1.5		ns
	t <sub>h</sub>	Minimum hold time, D after CLK $\uparrow$	1		ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low	3.3		ns
821	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q	6.7		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to Q	6.3		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to Q	6.7		ns
	t <sub>su</sub>	Minimum setup time, D before CLK $\uparrow$	2.1		ns
	t <sub>h</sub>	Minimum hold time, D after CLK $\uparrow$	1.3		ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low	3.8		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
823	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to Q	6.8		ns
	$t_{PHL}$	Maximum propagation delay, CLR to Q	7.1		
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	6.3		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	6.9		ns
	$t_{su}$	Minimum setup time, before CLK $\uparrow$	CLR inactive	2.5	ns
			Data	2.1	ns
			CLKEN low	3.3	ns
	$t_h$	Minimum hold time, after CLK $\uparrow$	Data	1.3	ns
			CLKEN low	2	ns
	$t_w$	Minimum pulse duration, CLK high or low	CLR low	5.5	ns
			CLK high or low	3.8	ns
841	$t_{PLH}$	Maximum propagation delay	D to Q	6.2	ns
	$t_{PHL}$	Maximum propagation delay	LE to Q	6.7	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	6.3		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	7.1		ns
	$t_{su}$	Minimum setup time, D before LE $\downarrow$	2.5		ns
	$t_h$	Minimum hold time, D after LE $\downarrow$	1.5		ns
	$t_w$	Minimum pulse duration, LE high	3.3		ns
843	$t_{PLH}$	Maximum propagation delay	D to Q	7.2	ns
	$t_{PHL}$	Maximum propagation delay	LE to Q	6.9	ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	PRE to Q	7.4	ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	CLR to Q	8	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	6.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	6.8		ns
	$t_{su}$	Minimum setup time, D before LE $\downarrow$	3		ns
	$t_h$	Minimum hold time, D after LE $\downarrow$	1		ns
	$t_w$	Minimum pulse duration	CLR low	5.5	ns
			PRE low	4.5	
			LE high	3.3	

Device	Symbol	Parameter	74 Series	54 Series	Units
16373	t <sub>PLH</sub>	Maximum propagation delay	D to Q	6.3	ns
	t <sub>PHL</sub>		LE to Q	6.7	ns
	t <sub>PZH</sub> t <sub>PZI</sub>	Maximum output enable delay, $\overline{G}$ to Q	6.1		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\overline{G}$ to Q	8.1		ns
	t <sub>su</sub>	Minimum setup time, D before LE↓	1.5		ns
	t <sub>h</sub>	Minimum hold time, D after LE↓	1		ns
	t <sub>w</sub>	Minimum pulse duration, LE high	3.3		ns
16374	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, CLK to Q	6.2		ns
	t <sub>PZH</sub> t <sub>PZI</sub>	Maximum output enable delay, $\overline{G}$ to Q	5.6		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\overline{G}$ to Q	8.2		ns
	t <sub>su</sub>	Minimum setup time, D before CLK↑	1.1		ns
	t <sub>h</sub>	Minimum hold time, D after CLK↑	1.3		ns
	t <sub>w</sub>	Minimum pulse duration, CLK high or low	3.3		ns

## 6.2.3 Transceivers:

Device	Symbol	Parameter	74 Series	54 Series	Units
245	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	4.6	4.8	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ to A or B	8.6	8.6	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ to A or B	8.8	8	ns
620	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	4.8		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}BA$ to A or $GAB$ to B	7.1		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ to A or $GAB$ to B	7		ns
623	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	4.6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}BA$ to A or $GAB$ to B	7.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ to A or $GAB$ to B	7.5		ns
640	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	4.9		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ to A or B	7.3		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ to A or B	8.8		ns
861	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	5.2		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}AB$ to B or $\overline{G}BA$ to A	6.9		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}AB$ to B or $\overline{G}BA$ to A	7.5		ns
863	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	6.3		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}AB$ to B or $\overline{G}BA$ to A	7.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}AB$ to B or $\overline{G}BA$ to A	7.1		ns
16245	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A or B to B or A	4.5		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ to A or B	7.2		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ to A or B	6.9		ns



## 6.2.4 Registered Transceivers:

Device	Symbol	Parameter	74 Series	'54 Series	Units
543	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A to B or B to A	6.9	ns
			$\overline{LEAB}$ or $\overline{LEBA}$ to B or A	7.1	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ or $\overline{CE}$ to A or B	7.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ or $\overline{CE}$ to A or B	8.4		ns
	$t_{su}$	Minimum setup time, A or B before $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	3.5		ns
	$t_h$	Minimum hold time, A or B after $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	2		ns
	$t_w$	Minimum pulse duration, $\overline{LE}$ or $\overline{CE}$ low	3.5		ns
544	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A to B or B to A	6.4	ns
			$\overline{LEAB}$ or $\overline{LEBA}$ to B or A	7.1	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ or $\overline{CE}$ to A or B	7.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ or $\overline{CE}$ to A or B	8.4		ns
	$t_{su}$	Minimum setup time, A or B before $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	3		ns
	$t_h$	Minimum hold time, A or B after $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	0.5		ns
	$t_w$	Minimum pulse duration, $\overline{LE}$ or $\overline{CE}$ low	3.5		ns
646	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A or B to B or A	6.9	ns
			CLKAB or CLKBA to B or A	8.4	ns
			SAB or SBA to B or A	8.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay	$\overline{G}$ to A or B	8.8	ns
			DIR to A or B	9.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay	$\overline{G}$ to A or B	8.8	ns
			DIR to A or B	9.5	ns
	$t_{su}$	Minimum setup time, A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	3.5		ns
	$t_h$	Minimum hold time, A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	1		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4		ns
648	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A or B to B or A	6.3	ns
			CLKAB or CLKBA to B or A	8.4	ns
			SAB or SBA to B or A	7.7	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay	$\overline{G}$ to A or B	8.8	ns
			DIR to A or B	9.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay	$\overline{G}$ to A or B	8.3	ns
			DIR to A or B	8.2	ns
	$t_{su}$	Minimum setup time, A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	3		ns
	$t_h$	Minimum hold time, A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	0		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
651	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A or B to B or A	6.2	ns
			CLKAB or CLKBA to B or A	5.6	ns
			SAB or SBA to B or A	6.5	ns
	$t_{PHL}$	Maximum output enable delay, $\overline{G}BA$ or $GAB$ to A or B	8.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ or $GAB$ to A or B	5.5		ns
	$t_{su}$	Minimum setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	3		ns
	$t_h$	Minimum hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	0		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4		ns
652	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A or B to B or A	6.7	ns
			CLKAB or CLKBA to B or A	8.4	ns
			SAB or SBA to B or A	7.7	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}BA$ or $GAB$ to A or B	8.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ or $GAB$ to A or B	8.2		ns
	$t_{su}$	Minimum setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	3.5		ns
	$t_h$	Minimum hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4		ns
2952	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLKBA or CLKAB to A or B	8.2		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}BA$ or $GAB$ to A or B	8.6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ or $GAB$ to A or B	8.1		ns
	$t_{su}$	Minimum setup time	A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	4.5	ns
			$\overline{CE}AB$ or $\overline{CE}BA$ before CLKAB $\uparrow$ or CLKBA $\uparrow$	4	ns
	$t_h$	Minimum hold time	A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1.5	ns
			$\overline{CE}AB$ or $\overline{CE}BA$ before CLKAB $\uparrow$ or CLKBA $\uparrow$	1.5	ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	3.5		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
2953	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLKBA or CLKAB to A or B	8.2		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{GBA}$ or $\overline{GAB}$ to A or B	8.6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{GBA}$ or $\overline{GAB}$ to A or B	8.1		ns
	$t_{su}$	Minimum setup time	A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	4	ns
			CEAB or CEBA before CLKAB $\uparrow$ or CLKBA $\uparrow$	3.5	ns
	$t_h$	Minimum hold time	A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	0	ns
			CEAB or CEBA after CLKAB $\uparrow$ or CLKBA $\uparrow$	0	ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	3.5		ns
16500	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, B or A to A or B	4.9		ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, LEBA or LEAB to A or B	5		ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, $\overline{CLKBA}$ or $\overline{CLKAB}$ to A or B	5.3		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{GBA}$ or $\overline{GAB}$ to A or B	5.6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{GBA}$ or $\overline{GAB}$ to A or B	6.5		ns
	$t_{su}$	Minimum setup time	A or B before $\overline{CLK}\uparrow$	4.5	ns
			A or B before LE $\downarrow$ (CLK high)	4.5	ns
			A or B before LE $\downarrow$ (CLK low)	4.5	ns
	$t_h$	Minimum hold time	A or B after $\overline{CLK}\uparrow$	0	ns
			A or B after LE $\downarrow$	2	ns
	$t_w$	Minimum pulse duration	LE high	3.3	ns
			$\overline{CLK}$ high or low	3.3	ns

Device	Symbol	Parameter	74 Series	54 Series	Units
16501	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, B or A to A or B	4.9		ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, LEBA or LEAB to A or B	5		ns
	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLKBA or CLKAB to A or B	5.5		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}B\overline{A}$ or GAB to A or B	5.6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}B\overline{A}$ or GAB to A or B	6.5		ns
	$t_{su}$	A or B before CLK $\uparrow$	4.5		ns
		A or B before LE $\downarrow$ (CLK high)	4.5		ns
		A or B before LE $\downarrow$ (CLK low)	4.5		ns
	$t_h$	A or B after CLK $\uparrow$	2		ns
		A or B after LE $\downarrow$	2		ns
	$t_w$	LE high	3.3		ns
		CLK high or low	3.3		ns
16543	$t_{PLH}$ $t_{PHL}$	A to B or B to A	5.7		ns
		LEAB or LEBA to B or A	5.6		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}$ or $\overline{CE}$ to A or B	7		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}$ or $\overline{CE}$ to A or B	6.3		ns
	$t_{su}$	Minimum setup time, A or B before LE $\uparrow$ or CE $\uparrow$	high		ns
		low	3.5		ns
	$t_h$	Minimum hold time, A or B after LE $\uparrow$ or CE $\uparrow$	high		ns
		low	2		ns
	$t_w$	Minimum pulse duration, LE or CE low	4		ns
16646	$t_{PLH}$ $t_{PHL}$	A or B to B or A	4.6		ns
		CLKAB or CLKBA to B or A	4.9		ns
		SAB or SBA to B or A	5		ns
	$t_{PZH}$ $t_{PZL}$	$\overline{G}$ to A or B	5.7		ns
		DIR to A or B	5.6		ns
	$t_{PHZ}$ $t_{PLZ}$	$\overline{G}$ to A or B	6		ns
		DIR to A or B	6.7		ns
	$t_{su}$	Minimum setup time, A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	3		ns
	$t_h$	Minimum hold time, A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	1		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4.3		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
16652	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	A or B to B or A	4.6	ns
			CLKAB or CLKBA to B or A	4.9	ns
			SAB or SBA to B or A	5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{G}BA$ or $GAB$ to A or B	5.5		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{G}BA$ or $GAB$ to A or B	6		ns
	$t_{su}$	Minimum setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	3		ns
	$t_h$	Minimum hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	4.3		ns
16952	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLKBA or CLKAB to A or B	5.3		ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\overline{OE}BA$ or $OEAB$ to A or B	6		ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\overline{OE}BA$ or $OEAB$ to A or B	6		ns
	$t_{su}$	Minimum setup time	A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	3.5	ns
			$\overline{CE}AB$ or $\overline{CE}BA$ before CLKAB $\uparrow$ or CLKBA $\uparrow$	3	ns
	$t_h$	Minimum hold time	A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1.5	ns
			$\overline{CE}AB$ or $\overline{CE}BA$ after CLKAB $\uparrow$ or CLKBA $\uparrow$	1.5	ns
	$t_w$	Minimum pulse duration, CLKAB or CLKBA	3.3		ns

## 6.2.5 Transceivers with Parity:

Device	Symbol	Parameter	74 Series	54 Series	Units
657	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay	A or B to B or A	5.5	ns
			A to PARITY	10.6	ns
			ODD/EVEN to PARITY	7.3	ns
			ODD/EVEN to ERROR	7.3	ns
			B to ERROR	14.5	ns
			PARITY to ERROR	9.4	ns
833	t <sub>PHL</sub>	Maximum output enable delay, G to A, B, PARITY, or ERROR	8.2		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G to A, B, PARITY, or ERROR	8.1		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A or B to B or A	5.3		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, G to A or B	6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G to A or B	7.6		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A or G to PARITY	10.8		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, G to PARITY	6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G to PARITY	7.6		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	CLK, CLR to ERR CLK to ERR	6.2		ns
	t <sub>su</sub>	Setup time before CLK↑	A port	9.8	ns
			CLR	3	ns
	t <sub>h</sub>	Hold time after CLK↑	A port	0	ns
	t <sub>w</sub>	Pulse duration	CLK	3	ns

Device	Symbol	Parameter	74 Series	54 Series	Units
853	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A or B to B or A	5.3		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to A or B	6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to A or B	8.1		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A to PARITY	11.2		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay $\bar{G}$ to PARITY	10.5		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to PARITY	6.7		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to PARITY	7.6		ns
	t <sub>PLH</sub>	CLR to ERR	6		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A, B or PARITY to ERR	12.8		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay LE to ERR	6.6		ns
	t <sub>su</sub>	Setup time before $\overline{LE} \downarrow$			
		A, B and PARITY	8.5		ns
	t <sub>h</sub>	Hold time after $\overline{LE} \downarrow$			
		CLR	2		ns
	t <sub>w</sub>	Pulse duration			
		LE high or low	3.5		ns
		CLR low	3.5		ns

Device	Symbol	Parameter	74 Series	54 Series	Units
899	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A or B to B or A	4.9		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A or B to BPAR or APAR	9.2		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay APAR or BPAR to BPAR or APAR	5.4		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay A, APAR, or B, BPAR to ERR $\bar{A}$ or ERR $\bar{B}$	8.5		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay ODD/EVEN to ERR $\bar{A}$ or ERR $\bar{B}$	7.3		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay ODD/EVEN to BPAR or APAR	7.8		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay SEL to BPAR or APAR	6		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay SEL to ERR $\bar{A}$ or ERR $\bar{B}$	12		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay LEAB OR LEBA to B or A	4.9		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay LEAB OR LEBA to BPAR or APAR (parity feed-through)	9.5		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay LEAB OR LEBA to BPAR or APAR (parity generated)	9.5		ns
	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay LEAB OR LEBA to ERR $\bar{B}$ or ERR $\bar{A}$	9.2		ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable time OEAB or OEBA to B or A	6		ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable time OEAB or OEBA to B or A	6		ns
	t <sub>su</sub>	Minimum setup time, D before LE $\downarrow$	2		ns
	t <sub>h</sub>	Minimum hold time, D after LE $\downarrow$	1.5		ns
	t <sub>w</sub>	Minimum pulse duration, LE high	3		ns



## **7 BC SWITCHING SPEED STANDARDS**

This section establishes standard maximum limits for switching parameters and minimum limits for timing parameters for the device types listed herein. For parameter measurement information, refer to Section 4.

Refer to individual manufacturers' datasheets for applicable minimum limits for switching parameters.

Standardized limits for switching parameters (dynamic characteristics) are specified by part identifiers in numeric order.

### **7.1 Index of BC device types:**

#### **7.1.1 Buffers and Drivers:**

230, 231, 240, 241, 244, 365, 366, 367, 368, 540, 541

#### **7.1.2 Latches and Flip-Flops:**

373, 374, 533, 534, 563, 564, 573, 574, 575

#### **7.1.3 Transceivers:**

242, 243, 620, 623, 640, 643, 645

## 7.2 BC Switching speed tables:

### 7.2.1 Buffers and Drivers:

Device	Symbol	Parameter	74 Series	Units
230	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
231	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, G or $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, G or $\bar{G}$ to Y	10	ns
240	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
241	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, G or $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, G or $\bar{G}$ to Y	10	ns
244	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
365	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
366	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
367	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns

Device	Symbol	Parameter	74 Series	Units
368	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
540	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns
541	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, A to Y	7.5	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Y	11	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Y	10	ns

## 7.2.2 Latches and Flip-Flops:

Device	Symbol	Parameter	74 Series	Units
373	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	D to Q 10	ns
			LE to Q 10	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	12.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	8.5	ns
	$t_{su}$	Minimum setup time, D before LE↓	2	ns
	$t_h$	Minimum hold time, D after LE↓	2	ns
	$t_w$	Minimum pulse duration, LE high	7	ns
374	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to Q	10	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	12.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	8.5	ns
	$t_{su}$	Minimum setup time, D before CLK↑	2	ns
	$t_h$	Minimum hold time, D after CLK↑	2	ns
	$t_w$	Minimum pulse duration, CLK high or low	7	ns
533	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	D to Q 10	ns
			LE to Q 10	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	12.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	8.5	ns
	$t_{su}$	Minimum setup time, D before LE↓	2.5	ns
	$t_h$	Minimum hold time, D after LE↓	2.5	ns
	$t_w$	Minimum pulse duration, LE high	7	ns
534	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to Q	10	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	12.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	8.5	ns
	$t_{su}$	Minimum setup time, D before CLK↑	2.5	ns
	$t_h$	Minimum hold time, D after CLK↑	2.5	ns
	$t_w$	Minimum pulse duration, CLK high or low	7	ns
563	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay	D to $\bar{Q}$ 13	ns
			LE to $\bar{Q}$ 13	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	14.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	10	ns
	$t_{su}$	Minimum setup time, D before LE↓	2.5	ns
	$t_h$	Minimum hold time, D after LE↓	2.5	ns
	$t_w$	Minimum pulse duration, LE high or low	7	ns

Device	Symbol	Parameter	74 Series	Units
564	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to $\bar{Q}$	13	ns
	$t_{PZH}$ $t_{PZI}$	Maximum output enable delay, $\bar{G}$ to $\bar{Q}$	14.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to $\bar{Q}$	10	ns
	$t_{su}$	Minimum setup time, D before CLK $\uparrow$	2.5	ns
	$t_h$	Minimum hold time, D after CLK $\uparrow$	2.5	ns
	$t_w$	Minimum pulse duration, CLK high or low	7	ns
573	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay D to $\bar{Q}$ LE to $\bar{Q}$	13 13	ns ns
	$t_{PZH}$ $t_{PZI}$	Maximum output enable delay, $\bar{G}$ to $\bar{Q}$	14.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to $\bar{Q}$	10	ns
	$t_{su}$	Minimum setup time, D before LE $\downarrow$	2	ns
	$t_h$	Minimum hold time, D after LE $\downarrow$	2	ns
	$t_w$	Minimum pulse duration, LE high or low	7	ns
574	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to $\bar{Q}$	10	ns
	$t_{PZH}$ $t_{PZI}$	Maximum output enable delay, $\bar{G}$ to $\bar{Q}$	12.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to $\bar{Q}$	8.5	ns
	$t_{su}$	Minimum setup time, D before CLK $\uparrow$	2	ns
	$t_h$	Minimum hold time, D after CLK $\uparrow$	2	ns
	$t_w$	Minimum pulse duration, CLK high or low	7	ns
575	$t_{PLH}$ $t_{PHL}$	Maximum propagation delay, CLK to Q	13	ns
	$t_{PZH}$ $t_{PZL}$	Maximum output enable delay, $\bar{G}$ to Q	14.5	ns
	$t_{PHZ}$ $t_{PLZ}$	Maximum output disable delay, $\bar{G}$ to Q	10	ns
	$t_{su}$	Minimum setup time, D before CLK $\downarrow$	2.5	ns
	$t_h$	Minimum hold time, D after CLK $\downarrow$	2.5	ns
	$t_w$	Minimum pulse duration, CLK high or low	7	ns

## 7.2.3 Transceivers:

Device	Symbol	Parameter	74 Series	Units
242	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	7.5	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, G or $\bar{G}$ to A or B	11.5	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G or $\bar{G}$ to A or B	10	ns
243	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	7.5	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, G or $\bar{G}$ to A or B	11.5	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G or $\bar{G}$ to A or B	10	ns
620	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	9.5	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, G or $\bar{G}$ to A or B	12.5	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, G or $\bar{G}$ to A or B	14	ns
623	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	8	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ A B to B or $\bar{G}$ B A to A	13	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ A B to B or $\bar{G}$ B A to A	13	ns
640	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	9.5	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to A or B	12.5	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to A or B	14	ns
643	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	9.5	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to A or B	13	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to A or B	14	ns
645	t <sub>PLH</sub> t <sub>PHL</sub>	Maximum propagation delay, A or B to B or A	8	ns
	t <sub>PZH</sub> t <sub>PZL</sub>	Maximum output enable delay, $\bar{G}$ to A or B	13	ns
	t <sub>PHZ</sub> t <sub>PLZ</sub>	Maximum output disable delay, $\bar{G}$ to A or B	13	ns